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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/730,321	FUKUSHIMA ET AL.	
	Examiner	Art Unit	
	Jasjit S. Vidwan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21,22 and 24-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21, 22 and 24-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments see Remarks, filed 7/11/07, with respect to the rejection(s) of claim(s) 21, 34, 40 under Thomann et al as modified by Pollard have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Thomann as modified by Huang.

2. Applicant's arguments with respect to remainder of the claims have been fully considered but they are not persuasive. Applicant argues that prior art of record fails to teach:

(a) Individually determining data transfer rates of each memory module; (Claim 31)

(b) "Based at least in part upon memory attribute information stored in the at least one memory module"; (Claim 35)

(c) "Determining a data transfer rate setting that is collectively applied to two memory modules based upon individually determined data transfer rate settings for each of the two memory modules" (Claim 36)

(d) "Locating data transfer rate setting values in a lookup table for memory modules" (Claim 38)

1. With respect to Argument (a), **Examiner disagrees**. Applicant argues that Thomann determines the data clock delay times for a system as a whole and not individually determine the clock delay for each DQ line. However, Thomann teaches a system wherein based on the memory module characteristics, either as Applicant alludes to, data clock cycle could be set for the system as a whole (i.e., all memory modules operate on same clock frequency) or each individual DQ line could have a separate data clock delay **[see Paragraph 0056, "In either instance, the characteristics of each memory device in the computer system must be known in order to select an appropriate data clock delay for each DQ line, for each memory device 100, or for the system as a whole."]**

2. With respect to Argument (b), **Examiner disagrees.** As was stated in the above response, the data clock cycle for each DQ line is set based on the characteristics of each memory device **[see above**

citation, Paragraph 0056, "..The characteristics of each memory device must be known in order to select appropriate data clock delay..."]

3. With respect to Argument (c), **Examiner disagrees**. It seems to the Examiner that the Applicant is contradicting himself from a point he made earlier in argument (a), wherein the Applicant argued that prior art teaches setting the data transfer rate collectively for all memory modules and was not capable of setting for individual memory modules. However, for Claim 36, Applicant argues that prior art (Pollard and Thomann) fail to teach determining a data transfer rate that is collectively applied to all memory modules based on individual characteristics. Examiner would like to direct Applicant's attention to above citation wherein Thomann teaches that either all memory modules could have different clock cycles or all maintain the same transfer rate based on characteristics from each individual memory module.

4. With respect to Argument (d), **Examiner disagrees**. Pollard teaches a system wherein after individual characteristics of each memory module has been retrieved, the system accesses lookup coefficients in a BIOS and using those coefficients calculates the data transfer rate for the memory module **[see Pollard, Col. 4, Lines 15-27]**. Though prior art might not teach retrieving a data transfer rate without any calculation from the lookup table, the limitations of Claim 38 do not require such teachings. In contrast, the claimed invention still requires "determining" the transfer rate from the lookup table. Therefore as claimed, the limitations do not exclude using a lookup table for influence coefficients and using those to further determine the transfer rate of the memory module.

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 21, 22, 24-40 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-15 of copending Application No. 10/730,319. Although the conflicting claims are not identical, they are not patentably distinct from each other because essentially the two applications claim similar subject matter outside of the fact that the present application deals with plurality of memory modules whereas the above mentioned copending application deals with a single memory module. However, the two applications are not patentably distinct because the method of claims in application 10/730,319 is identical to the method of setting the data transfer rate in the present application as well. One of ordinary skill in the art at the time of Applicant's invention would have been clearly motivated to apply the above teaching to the plurality of memory modules in order to maximize the performance of each individual memory while maintaining an overall balanced optimal temperature within the system.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 31, 32, 35-36 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomann et al U.S. Pub No: 2002/0169922 **[herein after Thomann]** and Pollard, II et al U.S. Patent No: 7,050,959 **[herein after Pollard].**

1. **As per Claim 31**, Thomann teaches a method for setting a data transfer rate **[Paragraph 0010, "...read/write timing calibration of these memory devices..."]** for multiple memory modules **[see Fig.**

1, element 30, "memory modules" – Though Fig. 1 is labeled as "prior art," Thomann teaches that his system may be used with any conventional memory architecture or computer system such as element 5 in figures 1-4 (all labeled "Prior art")] comprising processor **[see Fig. 1, element 10]** that is configured to execute the instructions in memory:

(a) Receiving memory module attribute information **[see Paragraph 0056, "Characteristics of each memory device"]** from each memory module in the multiple memory module **[Paragraph 0056, "In either instance, the characteristics of each memory device 100 in the computer system 5 must be known in order to select an appropriate data clock delay for each DQ line for each memory device 100 for each memory module 30 or for the system (i.e. all memory modules 30) as a whole"]**

(b) Individually determining data transfer rates **["Data clock delay" – see Paragraph 0054 – "Selection of the data clock delay is critical for high frequency applications, such as in the 300MHz to 500 MHz range, in order to provide optimum data transfer rates and to insure reliable data transfer."]** for each memory module in the multiple memory modules based at least in part upon the corresponding received memory module attribute information **[see Thomann, Paragraph 0063, "For DQ level calibration, read/write timing calibration is performed individually for all DQ lines on all memory modules 30 within the system"]**

(c) Collectively setting a data transfer rate with respect to the multiple memory modules based at least in part on the individually determined data transfer rates **[see Thomann, Paragraph 0063, "For device level calibration, a single data clock delay is selected to provide reliable data transfer on all DQ lines of a given memory device such that data transmission on any DQ line"]**

Thomann teaches the above limitations, however fails to explicitly state that memory module attribute information ("characteristics of each memory device") is received from attribute memories in each memory. Pollard of analogous art of setting data transfer rates based on certain characteristics of

individual memory module teaches the above limitation of storing the attribute information in the memory of each module **[See Pollard, Col. 5, Lines 30-37 - - Also see Fig. 2, elements 202 & 204]**.

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the teachings of Thomann with that of Pollard in order to take advantage of individually calculating the optimum power performance for each memory module based on its individual physical limitations (characteristics) rather than simply pre-selecting a "lowest" processing power whereby wasting valuable bandwidth and/or processing power **[see Col. 1, Lines 23-38]**. Therefore, it is for the above stated reason that one of ordinary skill would have been motivated to combine the teachings of Thomann with that of Pollard in order to maximize the physical limitations of every individual memory module within a system **[Col. 1, Lines 23-38]**.

2. **As per Claim 38**, Thomann as modified by Pollard above teaches a computer-readable medium comprising computer-executable instructions for:

(a) Acquiring memory attribute information **[see Thomann, Paragraph 0056, "Characteristics of each memory device"]** for each memory module in a plurality of memory modules **[see Thomann, Paragraph 0056, "In either instance, the characteristics of each memory device 100 in the computer system 5 must be known in order to select an appropriate data clock delay for each DQ line for each memory device 100 for each memory module 30 or for the system (i.e. all memory modules 30) as a whole"]**, wherein each of the memory modules include an attribute memory that retains the memory attribute information **[See Pollard, Col. 5, Lines 30-37 - - Also see Fig. 2, elements 202 & 204]**

(b) Accessing a setting value candidate database **[see Pollard, Col. 4, Lines 27-29, "Lookup table"]**

(c) Locating candidate data transfer rate setting values from each memory module in the plurality of memory modules in the setting value candidate database, wherein the candidate data transfer rate setting values correspond to the acquired memory attribute information in the setting value candidate database **[see Pollard, Col. 4, Lines 15-27 –**

The influence coefficients stored in BIOS 110 have major impact on determining the maximum sustainable power based on the acquired characteristics of the system including airflow rates, specific module layout and integrated circuit packaging - - System is similar to that of Thomann wherein the characteristics include operating voltage and operating temperature among other things (see Thomann, Paragraph 0055)].

(d) Determining a data transfer rate setting value that is to be applied with respect to each memory module in the plurality of memory modules based at least in part upon the located candidate data transfer rate setting values **[see Thomann, Paragraph 0063, "For device level calibration, a single data clock delay is selected to provide reliable data transfer on all DQ lines of a given memory device such that data transmission on any DQ line"]**

(e) Outputting the selected data transfer rate setting **["single data clock delay"]** value to a host controller that controls data transfer with respect to the plurality of memory modules **[see Thomann, Paragraph 0026, "The memory devices also receive one or more clock signals over the memory bus, the clock signals being provided by the processor, memory controller or another component of the computer system as desired"]**

3. **As per Claim 32,** Thomann and Pollard as modified by Huang teaches a method wherein collectively setting the data transfer rate with respect to the multiple memory modules comprises:

(a) Determining a maximum data transfer rate with respect to data transfer rates determined for each memory module **[see Pollard, Col. 4, Lines 46-57]**

(b) Determining a minimum data transfer rate with respect to data transfer rates determined for each memory module **[see Pollard, Col. 3, Lines 40-52]**

(c) Collectively setting the data transfer rate with respect to the multiple memory modules as a value that is between the maximum data transfer rate and the minimum data transfer rate **[see Pollard, Col. 5, Lines 4-9]**

3. **As per Claim 35**, see rejection of Claim 38 above

4. **As per Claim 36**, Thomann as modified by Pollard teaches an apparatus wherein the memory comprises additional instructions for:

(a) Acquiring a first and second upper limit temperature at which the first and second memory module is operated externally through a host controller **[see Pollard, Col. 3, Lines 30-40, "Maximum allowable junction temperature"]**

(b) Determining the first and second data transfer rate setting value based at least in part upon the first and second upper limit temperature **[see Pollard, Col. 3, Lines 40-48]**

4. Claims 21, 22, 24-27, 29, 34, 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomann et al U.S. Pub No: 2002/0169922 **[herein after Thomann]** and Pollard, II et al U.S. Patent No: 7,050,959 **[herein after Pollard]** further in view of Huang, U.S. Pub No: 2003/0095464 [herein after Huang]

5. **As per Claim 21**, Thomann teaches a method for setting a data transfer rate **[Paragraph 0010, "...read/write timing calibration of these memory devices..."]** for multiple memory modules **[see Fig. 1, element 30, "memory modules" – Though Fig. 1 is labeled as "prior art," Thomann teaches that his system may be used with any conventional memory architecture or computer system such as element 5 in figures 1-4 (all labeled "Prior art")]** comprising:

(a) Receiving memory module attribute information **[see Paragraph 0056, "Characteristics of each memory device"]** from each memory module in the multiple memory module **[Paragraph 0056, "In either instance, the characteristics of each memory device 100 in the computer system 5 must be known in order to select an**

appropriate data clock delay for each DQ line for each memory device 100 for each memory module 30 or for the system (i.e. all memory modules 30) as a whole"]

(b) Individually determining data transfer rates **["Data clock delay" – see Paragraph 0054 – "Selection of the data clock delay is critical for high frequency applications, such as in the 300MHz to 500 MHz range, in order to provide optimum data transfer rates and to insure reliable data transfer."]** for each memory module in the multiple memory modules based at least in part upon the corresponding received memory module attribute information **[see Thomann, Paragraph 0063, "For DQ level calibration, read/write timing calibration is performed individually for all DQ lines on all memory modules 30 within the system"]**

(c) Collectively setting a data transfer rate with respect to the multiple memory modules based at least in part on the individually determined data transfer rates **[see Thomann, Paragraph 0063, "For device level calibration, a single data clock delay is selected to provide reliable data transfer on all DQ lines of a given memory device such that data transmission on any DQ line"]**

Thomann teaches the above limitations, however fails to explicitly state that memory module attribute information ("characteristics of each memory device") is received from attribute memories in each memory. Pollard of analogous art of setting data transfer rates based on certain characteristics of individual memory module teaches the above limitation of storing the attribute information in the memory of each module **[See Pollard, Col. 5, Lines 30-37 - - Also see Fig. 2, elements 202 & 204]**.

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the teachings of Thomann with that of Pollard in order to take advantage of individually calculating the optimum power performance for each memory module based on its individual physical limitations (characteristics) rather than simply pre-selecting a "lowest" processing power whereby wasting valuable bandwidth and/or processing power **[see Col. 1, Lines 23-38]**. Therefore, it is for the above stated reason that one of ordinary skill would have been motivated to combine the teachings of Thomann

with that of Pollard in order to maximize the physical limitations of every individual memory module within a system **[Col. 1, Lines 23-38]**.

Thomann and Pollard above fail to teach a system wherein memory module attribute information includes position wherein the memory slot the said memory modules are located and based on this information to determine what transfer rate to apply. Huang of analogous art teaches the above limitation of determining which memory location the memory modules is located and applying transfer cycle rate to the said memory modules accordingly **[see Huang, Paragraph 0026]**.

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the above teachings in order to take advantage of providing different rates according to the distance between the control chipset and each memory unit so that memory access may attain an optimum efficiency **[see Huang, Paragraph 0022]**.

6. **As per Claim 22**, Thomann and Pollard as modified by Huang above teaches a method further comprising receiving an upper limit temperature at which each memory module in the multiple memory modules is operated **[see Thomann, Paragraph 055, "operating temperature" / also see Pollard Col. 3, Lines 30-39, "maximum allowable junction temperature"]**, wherein the data transfer rates are individually determined for each memory module in the multiple memory modules based at least in part upon the received upper limit temperature **[see Thomann, Paragraph 0063, "For DQ level calibration, read/write timing calibration is performed individually for all DQ lines on all memory modules 30 within the system"]**

7. **As per Claim 34 and 40**, see rejection of Claim 21

8. **As per Claim 24**, Thomann and Pollard as modified by Huang above teaches a method wherein the data transfer rate set collectively for the multiple memory modules is an upper limit value of a data transfer rate **[see Pollard, Col. 4, Lines 46-57]** at which a host controller accesses one of the multiple memory modules relative to a maximum data transfer rate at which the host controller can access the one of the multiple memory modules **[see Thomann, Paragraph 0063, "For device level calibration, a**

single data clock delay is selected to provide reliable data transfer on all DQ lines of a given memory device such that data transmission on any DQ line"]

9. **As per Claim 25**, *Limitations of said claim have been addressed previously during rejection of Claim 38. Applicant is advised to refer to appropriate claim for citations for the above claim language.*

10. **As per Claim 26**, Thomann and Pollard as modified by Huang above teaches a method wherein determining data transfer rates individually for each memory module in the multiple memory modules further comprises retrieving data transfer rates from the setting value candidate database for each memory module in the multiple memory modules **[see Thomann, Paragraph 0063]**, the data transfer rates from the setting value candidate database are located based at least in part upon memory attribute information stored in each of the memory modules respectively **[see Pollard, Col. 3, Lines 30-40]**

11. **As per Claim 27,** Thomann and Pollard as modified by Huang teaches a method wherein collectively setting the data transfer rate with respect to the multiple memory modules comprises:

(a) Determining a maximum data transfer rate with respect to data transfer rates determined for each memory module **[see Pollard, Col. 4, Lines 46-57]**

(b) Determining a minimum data transfer rate with respect to data transfer rates determined for each memory module **[see Pollard, Col. 3, Lines 40-52]**

(c) Collectively setting the data transfer rate with respect to the multiple memory modules as a value that is between the maximum data transfer rate and the minimum data transfer rate **[see Pollard, Col. 5, Lines 4-9]**

12. **As per Claim 29**, Thomann and Pollard as modified by Huang teaches a method wherein setting a data transfer rate with respect to the multiple memory modules collectively comprises transferring the data transfer rate with respect to the multiple memory modules to a host controller **[see Thomann, Paragraph 0026, "The memory devices also receive one or more clock signals over the memory bus, the clock signals being provided by the processor, memory controller or another component of the computer system as desired"]**

13. Claims 28, 33 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomann and Pollard and further in view of Mylly, U.S Pub No: 2005/0235110 **[herein after Mylly]**.

14. **As per Claim 28, 33 and 39**, Thomann and Pollard teach the limitations of Claims 21, 31 and 38, however fail to teach a method wherein collectively setting the data transfer rate with respect to the multiple memory modules comprises determining a minimum data transfer rate with respect to data transfer rates determined for each memory module and using the minimum data transfer rate as the collective data transfer rate for the multiple memory modules. Mylly, in an analogous art of setting data transfer rate of memory modules, teaches the above missing limitation of a method wherein collectively setting the data transfer rate with respect to the multiple memory modules comprises determining a minimum data transfer rate with respect to data transfer rates determined for each memory module **[see Mylly, Page 7, Paragraph 0105, "communication property information of low values – lowest performance limits of connected memory modules"]** and using the minimum data transfer rate as the collective data transfer rate for the multiple memory modules **[Page 4, Paragraph 0059, "...data transfer bus may be operated by a default setting of the communication properties in order to allow the communication with all connected memory modules (default setting comprise low clock frequency)"]**.

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the teachings above in order to take advantage of making sure that at a minimum, all connected memory modules are able to operate and no single memory module is handicapped by a unsustainable clock frequency **[see Paragraph 0055]**. It is for this reason that one of ordinary skill in the art at the time of Applicant's invention would have been motivated to combine the teachings above to take advantage of making sure that at a minimum, all connected memory modules are able to operate and no single memory module is handicapped by a unsustainable clock frequency **[see Paragraph 0055].**

15. Claims 30, 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomann and Pollard and further in view of Jeddeloh, U.S. Pub No: 2002/0144173 **[herein after Jeddeloh]**.

16. **As per Claim 37**, Thomann as modified by Pollard teach the limitations of Claim 31, however fail to teach a system wherein the acquired first memory attribute information and the acquired second

memory attribute information include serial presence detect information. Jeddeloh, of analogous art in setting memory module data transfer speeds, teaches the above missing limitation of having a system wherein the acquired first memory attribute information and the acquired second memory attribute information include serial presence detect information **[see Page 1, Paragraph 0005]**.

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the above teachings in order to take advantage of having a memory controller that selects the speed of the memory address/data bus and memory clock based on data identifying memory components which are stored in serial presence detect EEPROM **[see Jeddeloh, Paragraph 0006]**. It is for this reason that one of ordinary skill in the art at the time of Applicant's invention would have been motivated to combine the above teachings in order to take advantage of having a memory controller that selects the speed of the memory address/data bus and memory clock based on data identifying memory components which are stored in serial presence detect EEPROM **[see Jeddeloh, Paragraph 0006]**.

17. **As per Claim 30**, Thomann and Pollard as modified by Jeddeloh above teaches a method wherein the attribute information within at least one memory module of the multiple memory modules includes manufacturer identification information that indicates a manufacturer of the at least one memory module **[see Jeddeloh, Page 3, Claim 6]** number of devices information that indicates a number of devices on the at least one memory module **[see Jeddeloh, Page 3, Claim 4, "...the number of components in each said memory module"]**, memory bank information that indicates whether the at least one memory module is of a single-sided or of a double sided implementation **[see Thomann, Paragraph 0023, "Single in-line memory module ("SIMM") or dual in-line memory module ("DIMM")"]** and type identification information that identifies a type of the at least one memory module **[see Jeddeloh, Paragraph 0032, "type of memory module"]**

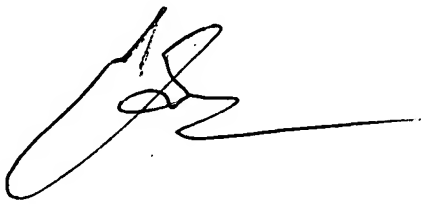
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasjit S. Vidwan whose telephone number is (571) 272-7936. The examiner can normally be reached on 8am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KIM HUYNH can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JSV
9/14/07



KIM HUYNH
SUPERVISORY PATENT EXAMINER

9/17/07